C2 cont.

16. The method according to claim 15, wherein:

said causing the processor to provide information about processor activity includes providing an indication every time the processor stalls that the processor has stalled.

17. The method according to claim 15, wherein:

the information about processor activity includes an indication of at least one of whether the last instruction executed was a jump, a jump based on the contents of a register, a branch taken, or an instruction which encountered an exception.

18. The method according to claim 15, further comprising:

c) providing information regarding the status of the processor when certain processor events occur, said certain processor events including at least one of a change in status of an interrupt line, an internal processor exception, and the execution of a jump instruction based on the contents of a register.

REMARKS

Pending claims 1-3 have been canceled and replaced with new claims 4-18. Claims 4, 9, and 15 are independent. Independent claim 4 is directed to a debugging method where information is provided on substantially every instruction executed. Independent claim 9 is directed to a method of debugging where the debugger

and the processor run on separate clocks. Independent claim 15 is directed to a method of debugging where the processor provides information about processor activity and the debugger associates the information with instructions executed.

Seagars et al. discloses a debugger interface unit for a data processing apparatus.

Seagars et al. does not teach or suggest providing information about substantially every instruction as claimed in claim 4. Seagars et al. only discloses providing information about breakpoint instructions to selected exception routines.

Seagars et al. does not teach or suggest providing a processor and a debugger with separate clocks as claimed in claim 9. Only a single clock is discussed in Seagars et al.

Seagars et al. does not teach or suggest a debugging method where the processor provides information about processor activity and the debugger associates this information with instructions as claimed in claim 15. In Seagars et al. the debugger merely sets a breakpoint register and an exception routine field.

Thus, none of the independent claims is anticipated or rendered obvious by Seagars et al.

Folwell et al. discloses a branch decision encoding scheme. Folwell et al. does not supply the teachings missing from Seagars et al. and described above. Thus, none of the independent claims is anticipated or rendered obvious by Folwell et al. taken alone or in combination with Seagars et al.

In light of all of the above, it is submitted that the claims are in order for allowance, and prompt allowance is earnestly requested. Should any issues remain outstanding, the Examiner is invited to call the undersigned attorney of record so that the case may proceed expeditiously to allowance.

Respectfully submitted,

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--This application is a continuation of U.S. Serial No. 09/064,474, filed April 22, 1998, now U.S. Patent Number 6,231,331 which is hereby incorporated by reference herein in its entirety.--